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EXAMINER	
YAM, STEPHEN K	

ART UNIT	PAPER NUMBER
2878	

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Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/813,073	OLSEN ET AL.	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group V, claims 30-84 in the reply filed on November 30, 2005 is acknowledged.

Claim Objections

2. Claim 68 is objected to because of the following informalities:

In Claim 68, line 10, "; and" should be replaced with a period.

Appropriate correction is required.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the storage node as part of the photodetector (recited in Claim 33) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The specification does not disclose the storage node as part of the photodetector as recited in Claim 33.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 30, 33-38, 40, 42, 68-73, 75, and 76 are rejected under 35 U.S.C. 102(e) as being anticipated by Henderson US Patent No. 6,952,004.

Regarding Claim 30, Henderson teaches (see Fig. 1a, 1b) a pixel circuit comprising a photodetector (22) that generates charge, a storage node (either Vpix or connection between transfer gate 14 and photodetector 22) for receiving charge generated by said photodetector (see Col. 2, lines 38-40), an amplifier (36) having an input coupled to said storage node (see Fig. 1b) and an output (Vout) that provides an amplified input signal (see Col. 2, lines 38-44), a feedback capacitor (Ch), said capacitor providing feedback between the amplifier's output and input (see Fig. 1b), and a reset switch (16) that resets said storage node when closed (see Col. 2, lines 25-29).

Regarding Claim 68, Henderson teaches (see Fig. 1a, 1b) an imaging circuit comprising an array of pixels (see Col. 2, lines 4-6), each pixel including a photodetector (22) that generates charge in response to light, a storage node (Vpix) for storing charges generated by said photodetector (see Col. 2, lines 38-40), an amplifier (36) that amplifies a signal received from said storage node (see Col. 2, lines 38-44), a feedback capacitor (Ch) that provides feedback to an input of the amplifier (see Fig. 1b), and a reset switch (16) that resets a storage node when closed (see Col. 2, lines 25-29).

Regarding Claim 75, Henderson teaches (see Fig. 1a, 1b) a pixel sensor array (see Col. 2, lines 3-5), comprising an array of pixel cells (10), each pixel cell including a photodetector (22) that generates charge in response to light, an amplifier (36) that amplifies a signal received from said photodetector (see Col. 2, lines 38-44), a feedback capacitor (Ch) that provides feedback to

the input of the amplifier (see Fig. 1a, 1b), and a reset switch (16) that resets the photodetector from a reset voltage line when closed (see Col. 2, lines 28-30).

Regarding Claim 33, Henderson teaches said storage node (connection between 14 and 22) as part of the photodetector (as charges accumulated on the photodetector 22 are stored on the photodetector when the transfer gate is open)

Regarding Claim 34, Henderson teaches said storage node (Vpix) as a floating diffusion node separate from said photodetector (see Fig. 1b and Col. 1, lines 22-27).

Regarding Claim 35, Henderson teaches said reset switch resets said feedback capacitor when closed (see Fig. 1B).

Regarding Claim 36, Henderson teaches said reset switch resets said photodetector from a reset voltage line (VRT) when closed (see Fig. 1b).

Regarding Claim 37, Henderson teaches a select switch (18), said select switch connecting the amplifier output (see Fig. 1a) to a column line when closed (30).

Regarding Claim 38, Henderson teaches an output stage (12) of said amplifier resides outside of a pixel array (see Fig. 1a).

Regarding Claim 40, Henderson teaches a transfer transistor (14) that transfers said charge from said photodetector to said amplifier (see Fig. 1a and 1b).

Regarding Claim 42, Henderson teaches a reset transistor (16) that resets said photodetector and said feedback capacitor (see Fig. 1a, 1b, and Col. 2, lines 26-37, 59-61).

Regarding Claim 69, Henderson teaches said amplifier as a capacitive transimpedance amplifier (see Fig. 1b).

Regarding Claim 70, Henderson teaches at least a portion (12) of said amplifier is located outside said array of pixels (see Fig. 1a).

Regarding Claim 71, Henderson teaches the array further comprises, for each pixel cell, a first select switch (18 in Fig. 1a, READ in Fig. 1b) that connects said capacitor and said reset switch to the amplifier output circuit when closed (see Fig. 1b).

Regarding Claim 72, Henderson teaches the array further comprises, for each pixel cell, a second select switch (16 in Fig. 1a, RESET in Fig. 1b) that connects the amplifier input to the amplifier output circuit when closed (see Fig. 1b).

Regarding Claim 73, Henderson teaches, for each pixel, a transfer transistor (14) that transfers charge from said photodetector to said amplifier (see Fig. 1b).

Regarding Claim 76, Henderson teaches each pixel cell further comprises a transfer transistor (14) that transfers charge from said photodetector to said amplifier (see Fig. 1a, 1b and Col. 2, lines 38-45).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 31-32, 39, 41, 62, 63, 74, 77, 78, and 80-84 are rejected under 35 U.S.C. 103(a) as being obvious over Henderson.

Regarding Claims 31-32, Henderson teaches the circuit in Claim 30, according to the appropriate paragraph above. Henderson also teaches a transfer transistor (14) that transfers said charge from said photodetector to said storage node (see Fig. 1a and 1b) and a power source (VRT) connected to said amplifier. Henderson does not teach a switch for selectively connecting one of a first and second power source to said amplifier. It is well known in the art to provide multiple reference/bias voltage levels through multiple power sources for connecting to an amplifier and to use a switch to select between multiple voltages, to provide adjustable operation of the amplifier. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a switch for selectively connecting one of a first and second power source to said amplifier, in the circuit of Henderson, as it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

Regarding Claim 77, Henderson teaches (see Fig. 1a, 1b) an imaging system comprising an imaging device (see Fig. 1a, 1b), the imaging device comprising an array (see Col. 2, lines 4-6) of pixels (10), each pixel including a photodetector (22) that generates charge in response to light, a storage node (either Vpix or connection between transfer gate 14 and photodetector 22) for storing charges generated by said photodetector, an amplifier (36) that amplifies charges on said storage node (see Col. 2, lines 38-44), a feedback capacitor (Ch) that provides feedback to an input of the amplifier (see Fig. 1b), and a reset switch (16) that resets the storage node when closed (see Col. 2, lines 26-29), and amplifier output circuitry (in (12)) (see Fig. 1a) located outside the pixel array, the amplifier, the amplifier output circuitry, and the feedback capacitor together forming a capacitive transimpedance amplifier (see Fig. 1b). Henderson does not teach

a processor coupled to the imaging device. It is well known in the art to provide processors in an imaging system coupled to an imaging array to process a received image for image optimization, scene recognition, auto-focusing, or other imaging purposes. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a processor coupled to the imaging device in the system of Henderson, to provide processing components of the output image for image analysis to accomplish an imaging task.

Regarding Claims 39, 74, and 80-82, Henderson teaches the circuit and system in Claims 30, 68, and 77, according to the appropriate paragraph above. Henderson does not teach the amplifier configured as a distributed folded four-transistor cascade amplifier, single ended four-transistor cascade amplifier, a folded four-transistor cascade amplifier, or a differential input telescopic cascade amplifier. It is well known in the art to select an appropriate amplifier type and configuration, depending on the desired operating characteristics of the circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the amplifier configured as a distributed folded four-transistor cascade amplifier, a single ended four-transistor cascade amplifier, a folded four-transistor cascade amplifier, or a differential input telescopic cascade amplifier in the circuit of Henderson, to provide components having the desired operating characteristics for optimal performance in the circuit.

Regarding Claim 41, Henderson teaches a switch circuit (18) that connects a pixel to a column line (30) (see Fig. 1a).

Regarding Claim 62 and 63, Henderson teaches the circuit in Claim 52, according to the appropriate paragraph above. Henderson does not teach the photodetector sensing visible light or infrared light. It is well known in the art to configure an imaging device to sense either visible

light or infrared light, depending on the desired application for the imaging device. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the photodetector sensing visible light or infrared light, in the device of Henderson, to provide appropriate detection characteristics for a specific desired imaging operation.

Regarding Claim 78, Henderson teaches each pixel comprising a first transfer transistor (14) that transfers said charge from said photodetector to said amplifier (see Fig. 1a and 1b).

Regarding Claim 83, Henderson teaches said storage node (connection between 14 and 22) as part of the photodetector (as charges accumulated on the photodetector 22 are stored on the photodetector when the transfer gate is open) and said reset switch resets said photodetector when closed (see Fig. 1b and Col. 2, lines 26-29).

Regarding Claim 84, Henderson teaches said storage node as a floating diffusion node (see Fig. 1b and Col. 1, lines 22-27) separate from said photodetector (see Fig. 1b) and said reset switch resets said floating diffusion node when closed (see Fig. 1b and Col. 2, lines 26-29).

9. Claims 41, 43-61, 64-67, and 79 are rejected under 35 U.S.C. 103(a) as being obvious over Henderson in view of Brehmer et al. US Patent No. 6,130,423.

Regarding Claims 43, 47, 50, 52, 67, and 79, Henderson teaches (see Fig. 1a, 1b) an integrated circuit comprising a pixel array (see Col. 2, lines 3-5) with rows and columns of pixel cells (10), and, for each column, a column readout line (30) that connects to the column's pixel cells (see Col. 2, lines 5-7, 15-18), each pixel cell including a photodetector (22) that provides a first signal indicating detected light, an amplifier (36) with an input (Vpix) that receives the first signal and an output (Vout) that provides an output signal based on the first signal, and feedback

capacitance (Ch) that provides feedback from the amplifier output to the amplifier input (see Fig. 1a, 1b), and readout circuitry (in (12)) connected to the column readout line. Regarding Claim 79, Henderson teaches the system in Claim 77, according to the appropriate paragraph above. Henderson does not teach the readout circuitry providing readout signals from the column pixel cells, the readout circuitry including sampling circuitry for sampling the amplifier output signal or the readout circuitry including amplifier output stage circuitry arranged such that when the pixel cell is connected to a column line the amplifier and the output stage circuitry form a distributed amplifier, or the amplifier including an input transistor and an output stage. Brehmer et al. teach (see Fig. 5 and 6) a similar integrated circuit with a pixel array (see Fig. 1) and for each column, a column readout line (690) that connects to the column's pixel cells (601), with each pixel cell having an amplifier (621, 625) and readout circuitry (in (602)) connected to the column readout line (see Fig. 6), the readout circuitry providing readout signals (690) from the column pixel cells (see Fig. 5 and 6), the readout circuitry including sampling circuitry (see Col. 6, lines 62-67) for sampling the amplifier output signal or the readout circuitry including amplifier output stage circuitry ((505) in Fig. 5, (602) in Fig. 6) arranged such that when the pixel cell is connected to a column line the amplifier and the output stage circuitry form a distributed amplifier (see Col. 4, lines 26-27 and Col. 5, lines 23-24), with the amplifier including an input transistor (621, 625) and an output stage (505/602). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the readout circuitry providing readout signals from the column pixel cells, the readout circuitry including sampling circuitry for sampling the amplifier output signal or the readout circuitry including amplifier output stage circuitry arranged such that when the pixel cell is connected to a

column line the amplifier and the output stage circuitry form a distributed amplifier, with the amplifier including an input transistor and an output stage, as taught by Brehmer et al., in the circuit of Henderson, to provide exposure and timing control for the image sensor for capturing an optimal image and to provide optimal signal amplification characteristics, as taught by Brehmer et al. (see Col. 1, lines 30-35).

Regarding Claims 44 and 58, Henderson teaches each pixel cell comprising a transfer transistor (14) that transfers said charge from said photodetector to said amplifier (see Fig. 1a and 1b).

Regarding Claim 45, Henderson teaches said amplifier selectively receives a reset signal and a charge generated signal at an input (based on correlated double sampling to obtain both an imaging signal and a reset signal for subtraction- see Col. 2, lines 46-52), said sampling circuitry obtaining a reset sample and a charge signal sample from said amplifier output (for the two output signals for correlated double sampling).

Regarding Claim 46, Henderson teaches the amplifier and feedback capacitor forming a capacitive transimpedance amplifier (see Fig. 1b)

Regarding Claims 48, 55-57, and 59-61, Henderson in view of Brehmer et al. teach the circuit in Claims 43 and 52, according to the appropriate paragraph above. Henderson does not teach the amplifier configured as a single ended four-transistor cascade amplifier, a folded four-transistor cascade amplifier, or a differential input telescopic cascade amplifier. It is well known in the art to select an appropriate amplifier type and configuration, depending on the desired operating characteristics of the circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the amplifier configured as a single ended four-

transistor cascade amplifier, a folded four-transistor cascade amplifier, or a differential input telescopic cascade amplifier in the circuit of Henderson in view of Brehmer et al., to provide components having the desired operating characteristics for optimal performance in the circuit.

Regarding Claim 41, Henderson teaches a switch circuit (18) that connects a pixel to a column line (30) (see Fig. 1a).

Regarding Claim 49, Henderson teaches a transfer transistor (14) that transfers said charge from said photodetector to said amplifier (see Fig. 1a and 1b).

Regarding Claim 51, Henderson in view of Brehmer et al. teach the circuit in Claim 43, according to the appropriate paragraph above. Henderson also teaches a power source (VRT) connected to said amplifier. Henderson does not teach a switch for selectively connecting one of a first and second power source to said amplifier. It is well known in the art to provide multiple reference/bias voltage levels through multiple power sources for connecting to an amplifier and to use a switch to select between multiple voltages, to provide adjustable operation of the amplifier. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a switch for selectively connecting one of a first and second power source to said amplifier, in the circuit of Henderson in view of Brehmer et al., as it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

Regarding Claim 53, Henderson teaches the output stage circuitry outside the pixel array (see Fig. 5 and 6).

Regarding Claim 54, Henderson teaches the pixel array further includes select circuitry (18) that connects a pixel cell to an associated column readout line in response to a row select signal (24) (see Col. 2, lines 3-18).

Regarding Claims 64 and 65, Henderson teaches each pixel cell further including a reset switch that, when closed, resets the photodetector and the amplifier to a reset level (see Col. 2, lines 26-29).

Regarding Claim 66, Henderson teaches each pixel cell further including a reset switch (16) that, when closed, resets the amplifier and a floating diffusion node (Vpix) (see Fig. 1b and Col. 1, lines 22-27) coupled to the photodetector and to the input of the amplifier (see Fig. 1b and Col. 2, lines 26-29).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571)272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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THANH X. LUU
PATENT EXAMINER